REMARKS

This Amendment responds to the Office Action dated January 26, 2005 in which the Examiner objected to the drawings and rejected claims 1-13 under 35 U.S.C. §102(e).

As indicated above, the claims have been amended to delete the term a spiral interconnection layer is formed on a semiconductor substrate with an interlayer insulating film therebetween. Therefore, Applicants respectfully request the Examiner withdraws the objection to the drawings.

Claims 1-13 were rejected under 35 U.S.C. §102(e) as being anticipated by *Muramatsu et al.* (U.S. Publication No. 2003/0146799).

Muramatsu et al. appears to disclose [0002] an enhanced voltage controlled oscillator that has an increased variable range of oscillation frequency. [0037] FIG. 2 is a circuit diagram showing a voltage controlled oscillator according to the first embodiment. [0038] In this embodiment, there are provided four switches SW1 to SW4 connected each at one end thereof to a constant current power supply 1. The other ends of the switches SW1 and SW2 are connected to one ends of inductors L1 and L2, respectively. The inductors L1 and L2 are equal to each other in inductance. The other ends of the switches SW3 and SW4 are connected to the inductors L1 and L2 at their midpoint positions, respectively. The inductance of the inductor L1 between the switches SW1 and SW3 is equal to that of the inductor L2 between the switches SW2 and SW4. [0039] The other end of the inductor L1 is connected with a varactor diode D1, the drain of a P-channel transistor Tr1, and the gate of a P-channel transistor Tr2, while the other end of the inductor L2 is connected with a varactor diode D2, the drain of the P-channel transistor Tr2, and the gate of the P-

channel transistor Tr1. An analog control voltage Vtune is applied to the varactor diodes D1 and D2, and a power supply voltage VDD is supplied to the sources of the P-channel transistors Tr1 and Tr2. [0046] FIG. 4 is a layout of the voltage controlled oscillator according to the first embodiment. [0047] Formed on a surface of a semiconductor substrate 11 are a diffusion layer 12 shared by the switches SW1 and SW2, a diffusion layer 13 for the switch SW1, a diffusion layer 14 for the switch SW2, a diffusion layer 15 shared by the switches SW3 and SW4, a diffusion layer 16 for the switch SW3, and a diffusion layer 17 for the switch SW4. The diffusion layer 12 is located between the diffusion layer 13 and the diffusion layer 14, while the diffusion layer 15 is located between the diffusion layer 16 and the diffusion layer 17. A gate insulating film 18 for the switch SW1 is formed between the diffusion layers 12 and 13 on the semiconductor substrate 11, while a gate insulating film 19 for the switch SW2 is formed between the diffusion layers 12 and 14 on the semiconductor substrate 11. A gate insulating film 20 for the switch SW3 is formed between the diffusion layers 15 and 16 on the semiconductor substrate 11, while a gate insulating film 21 for the switch SW4 is formed between the diffusion layers 15 and 17 on the semiconductor substrate 11. There are formed gate electrodes 22 to 25 on the gate insulating films 18 to 21, respectively.

Thus, *Muramatsu et al.* merely discloses four switches SW1-SW4 each connected at one end thereof to a constant current power supply 1 and the other ends of the switches connected to one end of inductors L1 and L2 respectively. Thus nothing in *Muramatsu et al.* shows, teaches or suggests second switch circuits having a first terminal connected to a first terminal of one of the plurality of first switch circuits and having a second terminal connected to the first terminal of

another one of the plurality of first switch circuits (i.e., the second switch circuits are connected in parallel with the first switch circuits) as claimed in claim 1. Rather, *Muramatsu et al.* merely discloses four switches connected at one end to a constant current power supply and the other ends connected to ends of the inductors. Applicant respectfully points out to the Examiner that selectively turning on the first and second switches as claimed in claim 1 allows precise control of inductance. In contrast, *Muramatsu et al.* is completely silent about the configuration to implement such fine control of inductance with inductor L2, and switches SW2 and SW4.

Also, *Muramatsu et al.* merely discloses inductors L1 and L2 formed of conductive spiral layers 38 and 39 [0048]. Nothing in *Muramatsu et al.* shows, teaches or suggests a plurality of spiral interconnection layers as claimed in claims 4 and 13. Rather, *Muramatsu et al.* only discloses a configuration where each of the inductors is formed of a single conductive layer.

Additionally, *Muramatsu et al.* merely discloses four switches SW1-SW4 and inductors L1, L2. Nothing in *Muramatsu et al.* shows, teaches or suggests a first switch circuit coupled between a first input/output terminals of first and second inductance variable portions and when the first switch circuit is turned on in response to a turn on of the second switch circuit, the first switch circuit electrically couples the first and second inductance variable portions as claimed in claim 7 and 8. Thus, as claimed in claims 7 and 8, the number of resistance components connected in series with the inductance element of each inductance variable portion is reduced and degradation in Q value of the LC resonant circuit is suppressed. Applicants respectfully submit that the switch circuits SW1-SW4 of *Muramatsu et al.* cannot

form a pair of inductors hindering reduction of resistance components of the inductance variable portion.

Finally, the voltage control oscillator of *Muramatsu et al.* is made of inductors L1, L2 and capacitance elements D1, D2. However, as claimed in claims 12 and 13, an L load differential circuit does not have a capacitance element connected between the first and second inductance variable portions. Thus nothing in *Muramatsu et al.* shows, teaches or suggests a first switch circuit coupled between the first input/output terminals of the first and second inductance variable portions and when the first switch circuit is turned on in response to a turn on of a second switch circuit, the first switch circuit electrically couples the first and second inductance variable portions as claimed in claims 12 and 13.

Since nothing in *Muramatsu et al.* shows, teaches or suggests the features as discussed above, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 4, 7, 8, 12 and 13 under 35 U.S.C. §102(e).

Claims 5-6 and 9-11 depend from claims 1 and 7 and recite additional features. Applicants respectfully submit that claims 5-6 and 9-11 would not have been anticipated by *Muramatsu et al.* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 5-6 and 9-11 under 35 U.S.C. §102(e).

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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